## REMARKS

This amendment is a full and timely response to the final Office Action of September 28, 2007. Reexamination and reconsideration are respectfully requested.

Applicant hereby renews and reiterates the arguments made in the Amendment filed July 24, 2007 and in the Request for Reconsideration filed November 6, 2007. In summary of those arguments, the cited references fail to teach two separate processors individually loading their respective instructions into a single common storage means.

The Advisory Action of November 27, 2007, appears to indicate a belief that, while neither reference teaches separately loading instructions into a common storage means, Sekizawa can be relied upon to teach separately loading instructions, while the AAPA can be relied upon to teach loading instructions into a common storage means. If the components of this feature are taken piecemeal from the references as suggested, there would not be a "reasonable expectation of success," as required to establish a *prima facie* case of obviousness.

The teachings of Sekizawa regarding separately loading instructions for separate processors into *separate* internal storage means is insufficient to teach one having ordinary skill in the art how to separately load instructions for separate processors into a *single* internal storage means. In the disclosure of Sekizawa, because each processor is provided with its own internal storage means, issues inherent to separately loading into a shared storage means, such as those disclosed in Applicant's specification, are not addressed at all.

The teachings of the AAPA regarding *simultaneously* loading instructions for separate processors into a single internal storage means is insufficient to teach one having ordinary skill in the art how to *separately* load instructions for separate processors into a single internal storage means. In the AAPA, because the instructions for all processors are combined into a single instruction block at compile time, issues inherent to separately loading into a shared storage means, such as those disclosed in Applicant's specification, are not addressed at all.

In other words, while a combination of the references may teach the individual concepts of "separately loading instructions" and "loading instructions into a single storage means," the combination would fail to teach one of ordinary skill in the art how to integrate these two concepts into a single step of separately loading instructions into a single storage means, as neither reference addresses how to solve the difficulties inherent to such an integration.

In an effort to advance the prosecution of this Application, claims 1, 3, 5, 7, 9, and 11 have been amended to further recite that "the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means." This recited feature further highlights the aspect of Applicant's invention that the prior art fails to teach, that is, combining separately loaded instructions into a single memory address space. The steps required for practicing this feature, shown for example in Applicant's Fig. 2, are not even suggested by either of the references. Without these additional teachings, a person having ordinary skill in the art could not have reasonably expected to be successful in practicing Applicant's invention.

For at least the above reasons, Applicant respectfully requests that the outstanding rejections under 35 U.S.C. § 103(a) be withdrawn. Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2802 from which the undersigned is authorized to draw.

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Respectfully submitted,

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